WHAT IS CLAIMED IS:

1. An apparatus for processing a data signal, comprising:

an acquisition unit of a test instrument for acquiring a data signal for a predetermined time;

a memory of said test instrument for storing said data signal;

a clock recovery unit for recovering a clock signal from said stored data signal; and

a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal.

2. The apparatus for processing a data signal of claim 1, wherein said clock recovery unit defines a threshold level relative to said stored data signal, compares each portion of the stored data signal to said threshold level, determines pairs of adjacent samples that straddle said threshold, and estimates a time of crossing said threshold between said adjacent samples to obtain a series of observed times of threshold crossing

3. The apparatus for processing a data signal of claim 2, wherein said threshold is defined as an absolute value.

4. The apparatus for processing a data signal of claim 2, wherein said threshold is defined as a percentage of said recorded data signal's amplitude.

5. The apparatus for processing a data signal of claim 2, wherein said clock recovery unit further considers a hysteresis requirement to confirm that a determined pair of adjacent samples that straddle said threshold should be included as part of said series of observed times of threshold crossing.

6. The apparatus for processing a data signal of claim 2, wherein each said time of crossing of said threshold is estimated based upon a linear interpolation.

7. The apparatus for processing a data signal of claim 2, wherein each said time of crossing of said threshold is estimated based upon a non-linear interpolation.

8. The apparatus for processing a data signal of claim 2, wherein said series of observed times of threshold crossing is used to obtain a recovered virtual periodic clock.

9. The apparatus for processing of claim 8, wherein said clock recovery unit compares said series of observed times of threshold crossing to an ideal perfectly periodic sequence of expected times of threshold crossing comprising said recovered virtual periodic clock, determines an error between said observed times and said expected times, and adjusts the phase of said recovered virtual periodic clock in accordance with said determined error.

10. The apparatus for processing of claim 8, wherein said clock recovery unit compares each element of said series of observed times of threshold crossing to each element of an ideal substantially periodic sequence of expected times of threshold crossing, determines the error between each observed time and the corresponding expected time, and based upon each error and preceding errors, adjusts the instantaneous phase of the substantially periodic sequence of times of threshold crossing according to mathematical algorithms thus obtaining a specified dynamic response for the recovered substantially periodic clock.

11. The apparatus for processing said data signal of claim 8, wherein said processor determines the absence of one or more transitions of said data signal, locates a position of a next transition of said data signal, and associates said located next transition of said data signal with a closest expected time of threshold crossing of said recovered virtual periodic clock.

12. The apparatus for processing said data signal of claim 8, wherein said processor determines a number of expected times of threshold crossing that have passed between two transitions of said data signal between which an absence of one or more transitions has been determined.

13. The apparatus for processing said data signal of claim 8, wherein said processor determines said expected transition times in accordance with calculations employing floating point numbers.

14. The apparatus for processing a data signal of claim 1, wherein the clock recovery unit estimates a frequency of said recovered clock, and discards a predetermined number of predicted times of threshold crossings of said data segments until said recovered clock settles to a substantially periodic frequency.

15. The apparatus for processing a data signal of claim 1, wherein the clock recovery unit detects a predetermined number of transitions of threshold crossings of said data segments, revises an initial phase of said recovered clock signal to give a mean time-error of zero for said predetermined number of transitions, and restarts processing.

16. The apparatus for processing a data signal of claim 15, wherein said recovered clock signal is made substantially perfectly periodic.

17. An apparatus for displaying an eye diagram, comprising:

an acquisition unit of a test instrument for acquiring a data signal for a predetermined time;

a memory of said test instrument for storing said data signal;

a clock recovery unit for recovering a clock signal from said stored data signal;

a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal; and

a display for overlaying said plurality of data segments in a time synchronized manner.

18. The apparatus for displaying an eye diagram of claim 17, wherein said display displays a second acquired data signal along with said first data signal.

19. The apparatus for displaying an eye diagram of claim 18, wherein said display displays said first and second data signal acquisitions after inter symbol interference processing.

20. The apparatus for displaying an eye diagram of claim 18, wherein said display displays said first and second data signal acquisitions after the data segments associated therewith are mathematically processed.

21. The apparatus for displaying an eye diagram of claim 17, wherein said clock recovery unit defines a vertical threshold relative to said stored data signal, compares each portion of the stored data signal to said vertical threshold, determines pairs of adjacent samples that straddle said vertical threshold, and estimates a time of crossing said vertical threshold between said adjacent samples to obtain a series of observed times of threshold crossing.

22. An apparatus for implementing a mask violation locator, comprising:

an acquisition unit of a test instrument for acquiring a data signal for a predetermined time;

a memory of said test instrument for storing said data signal;

a clock recovery unit for recovering a clock signal from said stored data signal;

a processor for slicing said stored data signal into a plurality of data segments of a predetermined length in accordance with said recovered clock signal;

a display for overlaying said plurality of data segments in a time synchronized manner to generate an eye diagram;

a mask definition unit for defining a portion of said display to constitute said mask; and

a determiner for determining whether one or more of said data segments violates said mask.

23. The apparatus of claim 22, wherein said clock recovery unit defines a vertical threshold relative to said stored data signal, compares each portion of the stored data signal to said vertical threshold, determines pairs of adjacent samples that straddle said threshold, and estimates a time of crossing said threshold between said adjacent samples to generate a series of expected times of threshold crossing.

24. The apparatus for implementing a mask violation locator of claim 22, wherein said first acquired data signal is discarded, but indications of any bits that violated said mask are retained upon acquisition of said second data signal.

25. The apparatus of claim 24, wherein when it is determined that one of said data segments violates said mask, said display displays a portion of said stored data signal including a portion thereof used to generate said data segment that violates said mask.

26. The apparatus of claim 24, wherein when it is determined a plurality of said data segments violate said mask, said processor stores a data segment identifier corresponding to each of said data segments determined to violate said mask, and said display displays, consecutively for each data segment corresponding to each data segment identifier, that portion of said stored data signal used to generate each of said data segments that violates said mask.